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Design of Energy Efficient SRAM Cell to Improve the Stability of Read Operation

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Abstract: Static Random Access Memory (SRAM) is a type of Memory which is faster and more suitable than other memories such as Dynamic Random Access Memory (DRAM) or Flash Memories. The main advantage of the SRAM is need not to be refreshed. SRAM is mainly used for Cache memory in many applications such as Microprocessors, Engineering Workstations, Mainframe Computers etc…for High Speed and Low Power Consumption. The Energy Efficiency and Speed of SRAM are the most Crucial issue for minimizing the power during read and write operations. The Aim of this Paper is to provide a Energy Efficient Low Power SRAM Cell and here Technique called "Self controllable voltage level circuits" are used and various Approaches are discussed to Achieve the Better Performance. Simulation result of 9T SRAM cell with reduced power is implemented using TANNER EDA tool.

Keywords: Static Random Access Memory (SRAM), Self Controllable Voltage Level Circuit (SVL), Energy Efficiency, Leakage, Low Power.

I.INTRODUCTION

System-on-chip refers to integrating all components of a computer or other Electronic System in to a Single Integrated circuit. It performs many functions on a Single Chip Substrate, some SOC's are used as Multiprocessor System-on-chip (MPSOC) which include more than one processor core. Usually Processor includes Memory Blocks such as ROM, RAM, EPROM, EEPROM and Flash.

From these blocks, SRAM plays a important role in Providing the Required Power, Performance and energy consumption of Applications and thereby Leakage is the main source of Energy Consumption, also the degradation of data stability in SRAM cells is another concern to be noted. SRAM's have achieved Ultra-Low Power Energy through Supply Scaling. Even though, they suffer from various design issues. By further scaling the Supply voltage near or below Transistor's threshold voltage, energy efficiency and power of SRAM will greatly affect the Performance.

Similarly other design Parameters such as Stability, read/write margin and leakage are noted for Reliable Performance. Generally, In CMOS Circuits the static leakage power affects the SRAM for two main reasons. First, Leakage Power is Proportional to total number of transistors on chip and secondly it is related to temperature dependence of some sources of Leakage Power. Hence in order to improve Leakage and to achieve Energy Efficiency, Techniques and approaches were discussed for new nine-transistor (9T) SRAM cell with Energy Efficient and enhanced data stability of Read operation.

II.EXISTING METHOD

SRAM consists of simple latch circuit with two stable operating points. The Nine transistor(9T) SRAM cell usually requires nine transistors per bit also and involves data access mechanisms for Read and Write operations.

The main critical issue in this method are Leakage power which affects all kinds of CMOS Circuits for two main reasons.

1.Leakage Power is proportional to total number of transistors on chip
2.Temperature dependence of some sources of leakage power

A.9T SRAM

The 9T SRAM Cell consists of 9T with two dynamic inverters which usually operate in various clock rates. The Voltage drop at the read bit line is very small due to leakage current.

B.9T SRAM CELL DESIGN

The 9T SRAM Cell comprises of N1,N2,N3,N4,N5,N6,N7,P1,P2 with W=Wmin and L=Lmin. N5 and N6 are bit line access transistors and N7 is the read access transistors. The N5 and N6 transistors are controlled by data stored in the cell.N7 is controlled by Read Signal (RD), Here the below figure represents the layout of 9T SRAM cell.

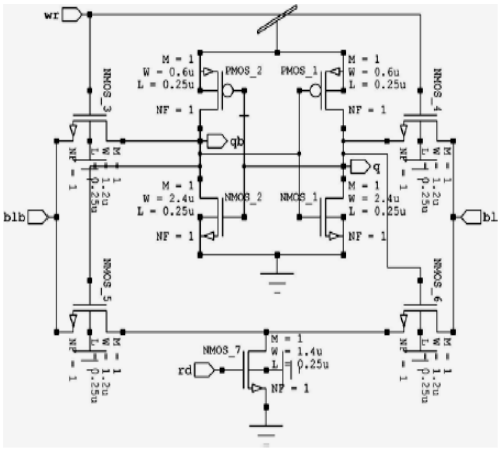

FIGURE 1: 9T SRAM CELL

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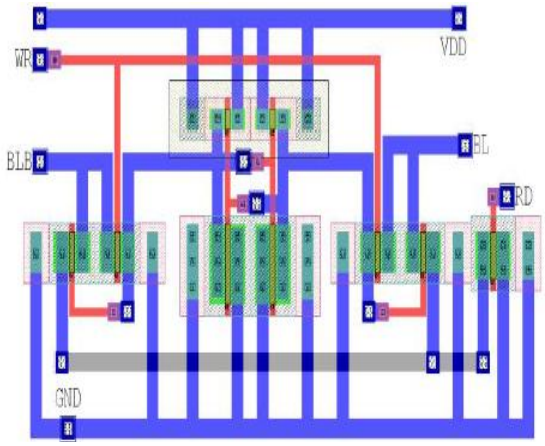

FIGURE 2: 9T SRAM CELL LAYOUT

C.WRITE OPERATION OF 9T SRAM CELL

While Write operation, RD is maintained Low and WR signal transitions are kept high. The transistors N3 and N4 are write access transistors and they are turned 'ON'. To write a '0' to Node 1, BL and BLB are discharged and charged simultaneously. A '0' is forced to Node 2 through N4 for writing '0' in Node 2.

The aspect ratio of pull up network of transistors N1 to access transistor N4 is called "Pull up ratio"

$$\text{Pull up ratio(PU)} = N1/N4$$

Where
N1 is the trans conductance of pull up transistor (p3)
N4 is the trans conductance of access transistor (N6)

The Parameter PU defines the write stability of SRAM cell.

D.READ OPERATION OF 9T SRAM CELL

While Read operation both BL and BLB are made high. To read '0', the transistors P1 and P2 is 'ON' state and voltage discharges through access transistors N3 through P1 and P2. To read '1', node BL is grounded and make transistors N1 and N2 as 'ON' state thereby voltage is discharged through access transistor N4 through N1 and N2.

The aspect ratio of pull down network of transistors N1 to access transistor N5 is called "Pull down ratio"

$$\text{Pull down ratio(PU)} = N1/N5$$

Where
N1 is the trans conductance of pull down transistor (N1)
N5 is the trans conductance of access transistor (N5)

The Parameter PU defines the write stability of SRAM cell.

III. PROPOSED METHOD

A.SELF-CONTROLLABLE VOLTAGE LEVEL CIRCUITS

A self-controllable voltage level circuit (SVL) can supply a large amount of DC voltage to an active load circuit while needed or can minimize the DC voltage supplied to the load circuit in standby mode. This circuit controls the effective voltage across the SRAM cell in inactive or idle mode , also they can suddenly reduce the standby leakage power of CMOS circuits with minimum overheads behalf of the standby mode.

Generally there are two techniques to reduce the leakage power. One is to use a multi-threshold voltage CMOS(MTCMOS), thus reduces the leakage power by disconnecting power supply through the V_t MOSFET switches. The main drawback of this technique were both memories and flip flops does not remain data. The other technique by using variable threshold voltage (VTCMOS) which reduces leakage power by increasing the substrate-biases and also it causes problem such as large area and large power due to substrate-bias supply circuits which requires low leakage power.

The main theme is that when the SRAM cell is in active mode then the capacitive leakage is low and no noise margin. While standby mode , the capacitive leakage is high and minimum supply voltage is given to the SRAM cell thereby reducing leakage current and noise margin.

B.IMPROVED SELFCONTROLLABLE VOLTAGE LEVEL CIRCUITS

I. UPPER SVL CIRCUIT

In Upper self-controllable voltage level circuit (SVL) the impedance of MOS transistor increases with the width of transistor. PMOS1 having width means it offers high resistance in the path between V_{dd} and V_d. The NMOS1 and NMOS2 form a read and write working in normal mode of a cell whereas NMOS2 act as resistor to reduce current in active mode by connecting upper SVL circuit and reduced leakage power.

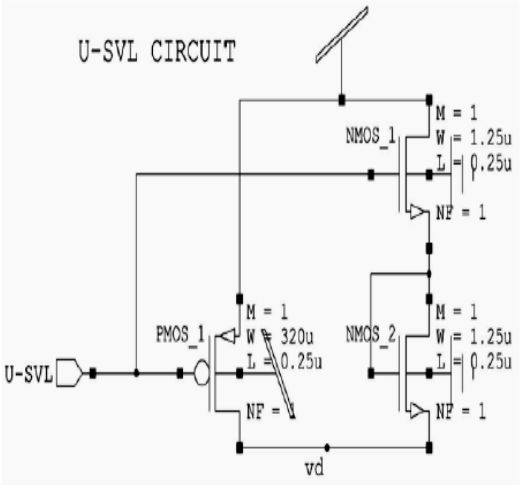

FIGURE 3 : UPPER SVL CIRCUIT

II. LOWER SVL CIRCUIT

In Lower self-controllable voltage level circuit (SVL) the impedance of MOS transistor increases with the width of transistor. NMOS1 having width means it offers high resistance in the path between V_{dd} and V_d.

The NMOS3 work in SVL mode and PMOS2 and PMOS3 work in normal mode of the cell. PMOS2 act as resistor to reduce leakage power. The lower SVL circuit not only supply power to active load circuit through the on n-SW and also supplies Vss to the standby load circuit through p-SWs.

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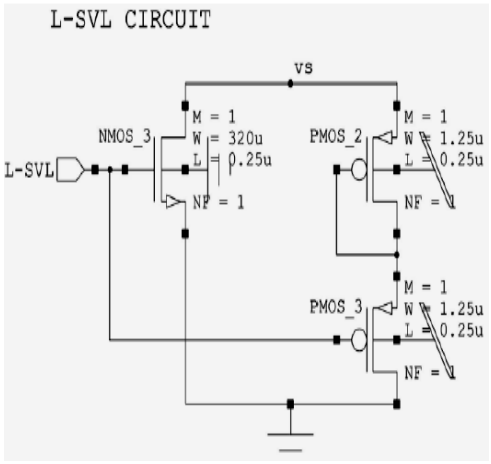

FIGURE 4 : LOWER SVL CIRCUIT

C. SRAM CELL WITH NORMAL SVL CIRCUITS

The role of SVL circuit is to reduce leakage current in standby mode or hold mode, hence maximum leakage power in stand by mode can destroy the cell. Thereby to reduce leakage proposed improved SVL circuits are built. Let us consider the u-svl as input '1' and l-svl as input '0' then the cell operates in Hold mode, in this mode nmos8 on upper SVL circuit and pmos4 on lower SVL circuit to reduce the leakage.

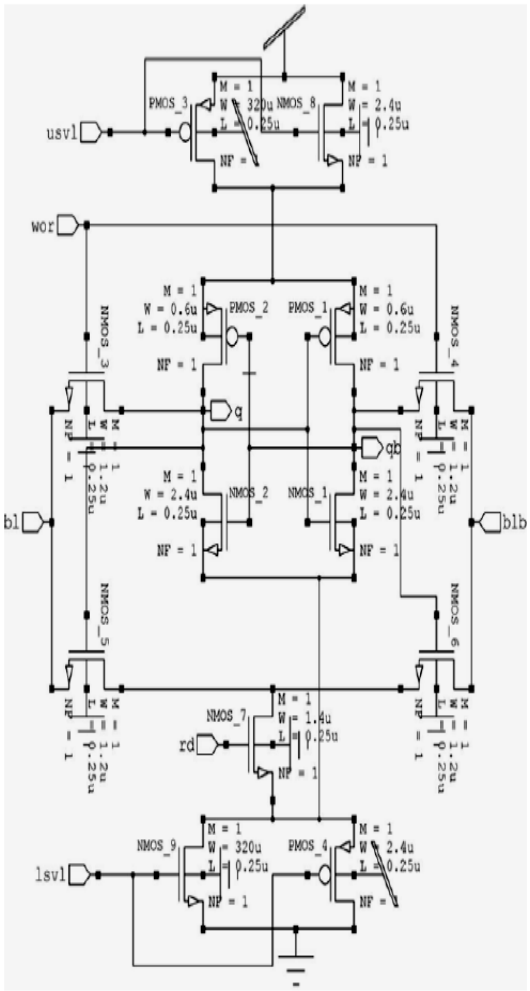

FIGURE 5: SRAM CELL WITH NORMAL SVL CIRCUIT

Simultaneously set u-svl as logic '0' and l-svl as logic '1' then the cell operates as Read operation, u-svl as logic '0' and l-svl as logic '0' then the cell operates as Write0 and u-svl as logic '0' and l-svl as logic '0' then the cell operates as Write1.

D. PROPOSED 9T SRAM CELL WITH IMPROVED SVL CIRCUITS

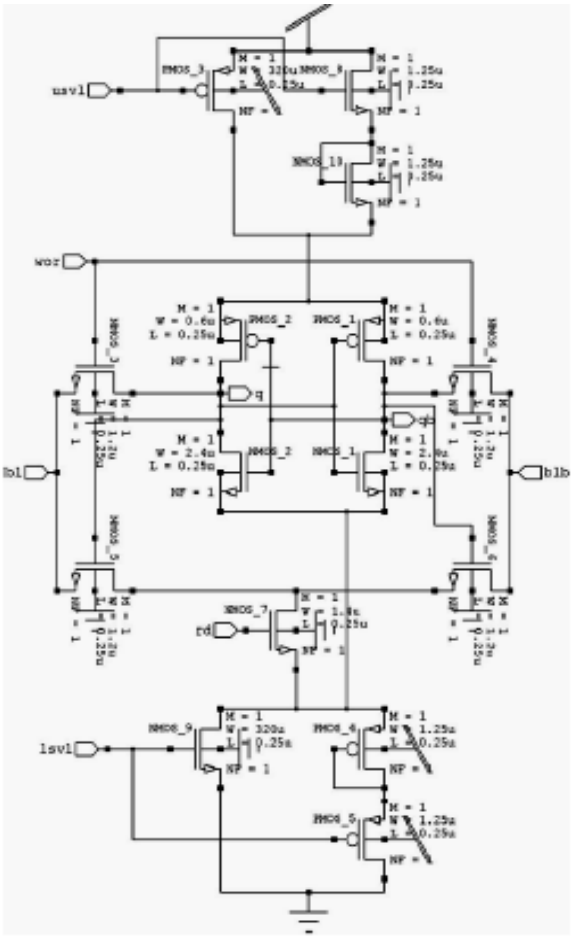

FIGURE 6 : SRAM CELL WITH IMPROVED SVL CIRCUITS

The proposed 9T SRAM cell with improved SVL circuits reduces the leakage power in standby mode to protect the cell as shown in below figure. NMOS9 and PMOS3 also reduces leakage and thereby improves the stability of read operation.

Further PMOS4 and NMOS10 is placed. In other modes the cell operates as normal operation read, write whereas the write mode has maximum noise margin and the read mode has minimum noise margin.

E.SIMULATION RESULTS

Simulation results are performed using Tanner EDA tool with supply voltage ranging from 5V and operating frequency of 50MHZ.To implement an impartial testing each circuit have been tested on the same input patterns.

The below waveform shows proposed 9T SRAM cell with improved self-controllable voltage level circuit for the inputs of wr, rd and bl and their corresponding outputs are q and qb.

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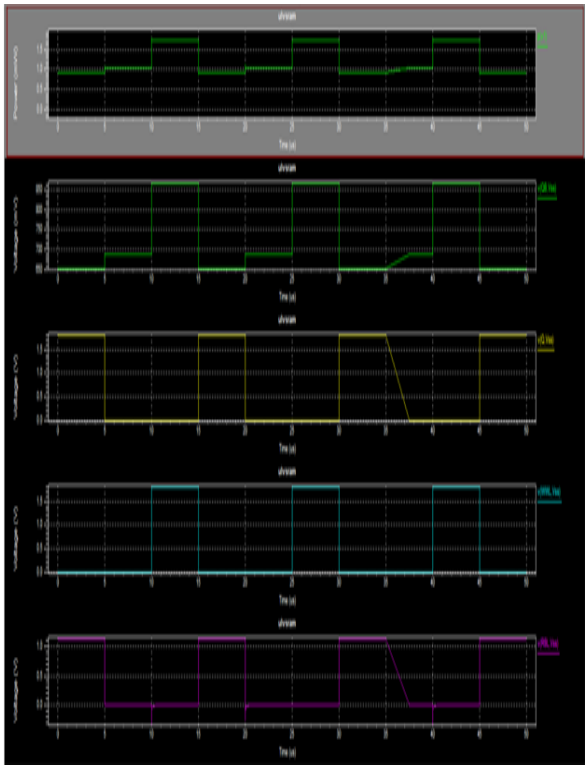

FIGURE 7 : OUTPUT WAVEFORM OF SRAM CELL WITH IMPROVED SVL CIRCUITS

F.PERFORMANCE ANALYSIS

Power , Delay and Number of transistors in SRAM with Normal SVL circuit and improved SVL circuit is compared in the below table.

SRAM	POWER	DELAY
9T SRAM with normal SVL	7.492e-004 watts	34.8ns
9T SRAM with improved SVL	4.49e-004 watts	50.3ns

IV. CONCLUSION

The effect of the improved SVL circuit shows the leakage current through the load circuit is described. The improved SVL circuit and load circuit were designed by using Tanner EDA tool. Sub-threshold memory design was noticed in various issues but most of them use large number of transistors and power to achieve sub threshold region operation. In this circuit we have several advantages in different modes that is in operating mode high drain to source voltage to load circuits and for high speed operation in stand-by-mode, high threshold voltage through load circuits for minimum stand-by leakage power, high noise immunity, stand-by power dissipation and delay. Because of the low cost and reduction of transistors the SVL method can be implemented also for DRAM in future.

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